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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,854	04/15/2004	Chien-Chao Huang	24061.150/TSM2003-0964	6844

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/824,854	HUANG ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *17-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004 and 11 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 04/11/2006 has been entered.

Drawings

2. The proposed replacement sheet of drawings, filed on 04/11/2006 has been approved.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 17-27 are rejected under 35 U.S.C. 102(e) as being anticipated by LIN AL. (2005/0224786).

Lin al. discloses a microelectronic device comprising a substrate 210-220 having a plurality 230a-b-c of doped regions therein, comprising diamond or strained silicon; a

patterned feature 240a-b, 260a-c located over the substrate 210-220 and over the plurality 230a-b-c of doped regions, the patterned feature 240a-b, 260a,b,c being part of a transistor (note paragraph 0026) and comprising at least one electrode 240a-260a or 240b-260b, the electrode 240a-260a or 240b-260b being situated proximate the plurality 230a-b-c of doped regions; and a silicon germanium or strained silicon comprising sill 260a or 260b, located within the electrode 240a-260a or 240b-260b, the sill 260a or 260b comprising at least one germanium-comprising impurity or at least two distinct and segregated impurities, and adapted for modifying an electrical property of at least one member 230a or 230b (sill 260a is adapted for modifying said electrical property of member 230a, by injecting current into said member; conversely sill 260b is adapted for modifying said electrical property of member 230b, by removing current from said member) adjacent the electrode 240a-260a or 240b-260b, and a second sill 260c comprising diamond; wherein the sill 260a or 260b is formed prior to the patterning of the electrode 240a-260a or 240b-260b or the sill 260a or 260b is formed in the electrode 240a-260a or 240b-260b, the electrode 240a-260a or 240b-260b and partially etched to reduce the thickness of the electrode 240a-260a or 240b-260b and the sill 260a or 260b, and wherein the electrode impurity concentration ranges between about 10^{13} atoms/cm^3 and about 10^{19} atoms/cm^3. Note figure 2 and paragraphs 0028-0030 of Lin al.

B. Claims 17-20 and 22-26 are rejected under 35 U.S.C. 102(e) as being anticipated by MONTGOMERY ET AL. (2004/0208454).

Montgomery et al. discloses a microelectronic device comprising a substrate 32-34-36 having a plurality 40-44 of doped regions therein, comprising strained silicon (note paragraph 0011); a patterned feature 22 located over the substrate 32-34-36 and over the plurality 40-44 of doped regions, the patterned feature 22 being part of a transistor (note, abstract, that patterned feature 22 includes a gate region to overly a body region, with a relatively thin dielectric layer interposed between the contiguous portions of the gate and body regions, to allow voltage imposed on the gate region, in order, note figure 18, to modulate current flowing from "source" contact 42-1 to "drain" contact 42-2. The gate, body, and relatively thin dielectric layer, as well as the ability to modulate a current with an applied voltage, identify the disclosed structure as a transistor) comprising at least one electrode 48-52-53, the electrode 48-52-53 being situated proximate the plurality 40-44 of doped regions; and a silicon germanium or strained silicon (note paragraph 0051) comprising sill 52, located within the electrode 48-52-53, the sill 52 comprising at least one germanium-comprising impurity or at least two distinct and segregated impurities, and adapted for modifying an electrical property of at least one member 230a or 230b adjacent the electrode 48-52-53; wherein the electrode impurity concentration ranges between about 10^{13} atoms/cm^3 and about 10^{19} atoms/cm^3. Note

figures 2-4,16,18,22, abstract, paragraphs 0051-0054, and paragraph 0067 of Montgomery et al.

The applicant's claims 18 and 19 do not distinguish over the Montgomery et al. reference regardless of the process used to form the sill and the electrode, because only the final product is relevant, not the recited processes of forming the sill prior to the patterning of the electrode or forming the sill in the electrode and partially etching the electrode to reduce the thickness of the electrode and the sill.

Response to Arguments

4. Applicant's arguments filed 04/11/2006 have been fully considered but they are not persuasive.

It is argued, at page 7 of the remarks, that "The foregoing amendments [changing 'a plurality of doped layers' to 'the plurality of doped regions'] implement the Examiner's proposed change to Claim 17. It is respectfully submitted that this change in Claim 17 cures the objection to Claim 17, and also cures the corresponding objections to the drawings and the specification. Notice to that effect is respectfully requested." The Examiner agrees that the change to claim 17 renders moot the objections to spec and drawings to which applicant refers.

It is argued, at page 7 of the remarks that "In contrast, the doped regions in Montgomery are not within the substrate 32." Montgomery et al. employ what is commonly called an SOI substrate. The SOI substrate is a three-part substrate identified with part #s 32, 34, and 36. In an SOI substrate, the practice is to dope only the top, or "semiconductor" portion, leaving undoped the lower, "substrate" (a term of art with reference to SOI substrates) and middle "oxide" layers.

It is argued, at page 7 of the remarks, that "Further, the device formed by Montgomery is an electro-optic modulator, and not a "transistor" as recited in Claim 17." As explained above, Montgomery et al.'s device includes a gate region to overly a body region, with a relatively thin dielectric layer interposed between the contiguous portions of the gate and body regions, to allow voltage imposed on the gate region to modulate (note figure 18) current flowing from "source" contact 42-1 to "drain" contact 42-2. The gate, body, and relatively thin dielectric layer, as well as the ability to modulate a current using an applied voltage, identify the disclosed structure as a transistor.

Lastly at page 7 it is argued that "Claim 17 of the present application expressly recites '. . . a sill located within the electrode . . .' Contrary to the assertions in the Office Action, the sill disclosed in Lin is not within an electrode."

However, during patent examination, the pending claims must be given their "broadest reasonable interpretation consistent with the specification." In re Hyatt, 21 1

F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). While the claims of issued patents are interpreted in light of the specification, prosecution history, prior art and other claims, this is not the mode of claim interpretation to be applied during examination. During examination, the claims must be interpreted as broadly as their terms reasonably allow. In re American Academy of Science Tech Center, WL 1067528 (Fed. Cir. May 13, 2004); In re Zletz, 893 F.2d 319, 321, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989); Chef America, Inc. v. Lamb-Weston, Inc., 358 F.3d 1371, 1372, 69 USPQ2d 1857 (Fed. Cir. 2004).

Applicants' specification and drawings show a two-part electrode consisting of contact 240c and sill 250a, for supplying charge to biasing feature 250 (Note that sill 250a "may" be formed inside feature 250, but "alternately" may be a plurality of layers formed on biasing feature 250). Note figure 2 and paragraphs 0030-0033 of the instant application. Lin et al. show the same two-part electrode (parts 240b and 260b in Lin et al.) for supplying current to semiconductor feature 230b. Note figure 2 of Lin et al. Given that we are mandated during examination to give Applicants' claims the broadest reasonable interpretation consistent with Applicants' disclosure (and given the close similarity between Lin's electrode 240b-260b and Applicants' disclosed electrode 240c-250a) it is impossible to conclude that Applicants' claimed electrode/sill combination is not met by the two-part electrode including a sill, as disclosed by Lin et al.

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thomas L. Dickey
Patent Examiner
Art Unit 2826
07/06